5049015640500

FIG. 1

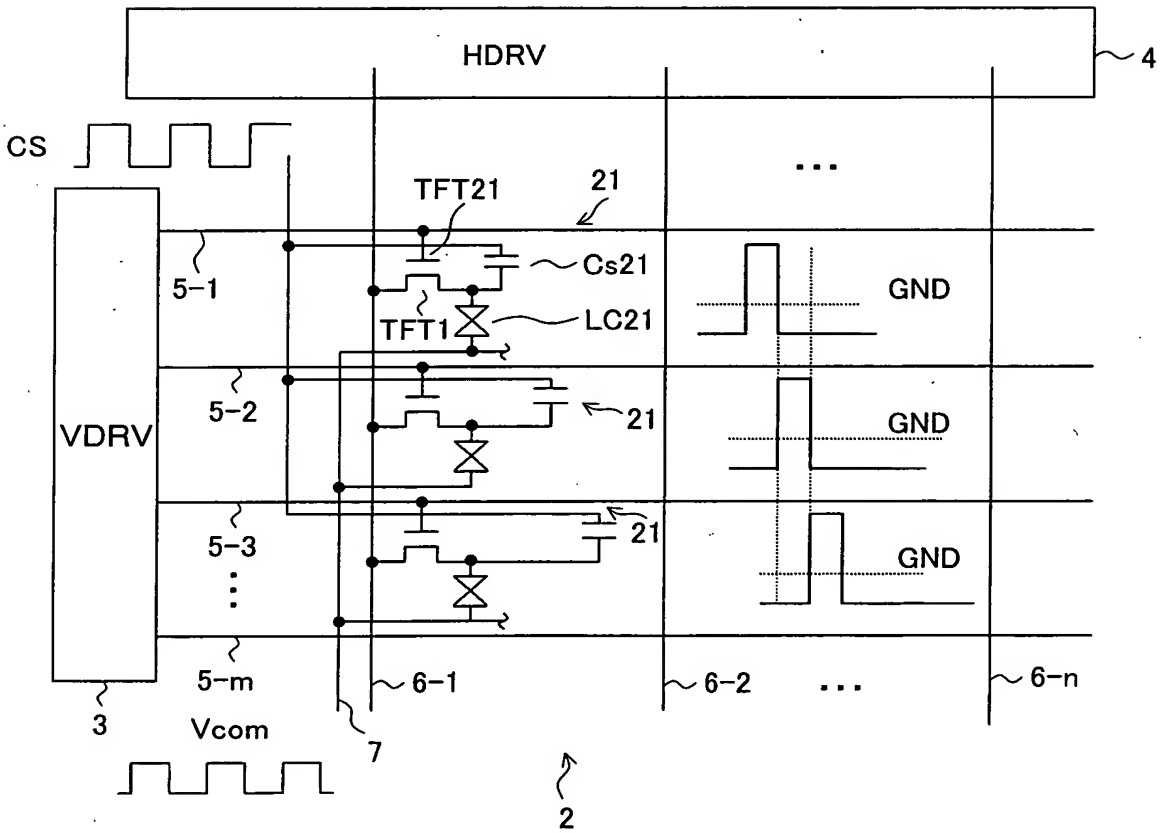
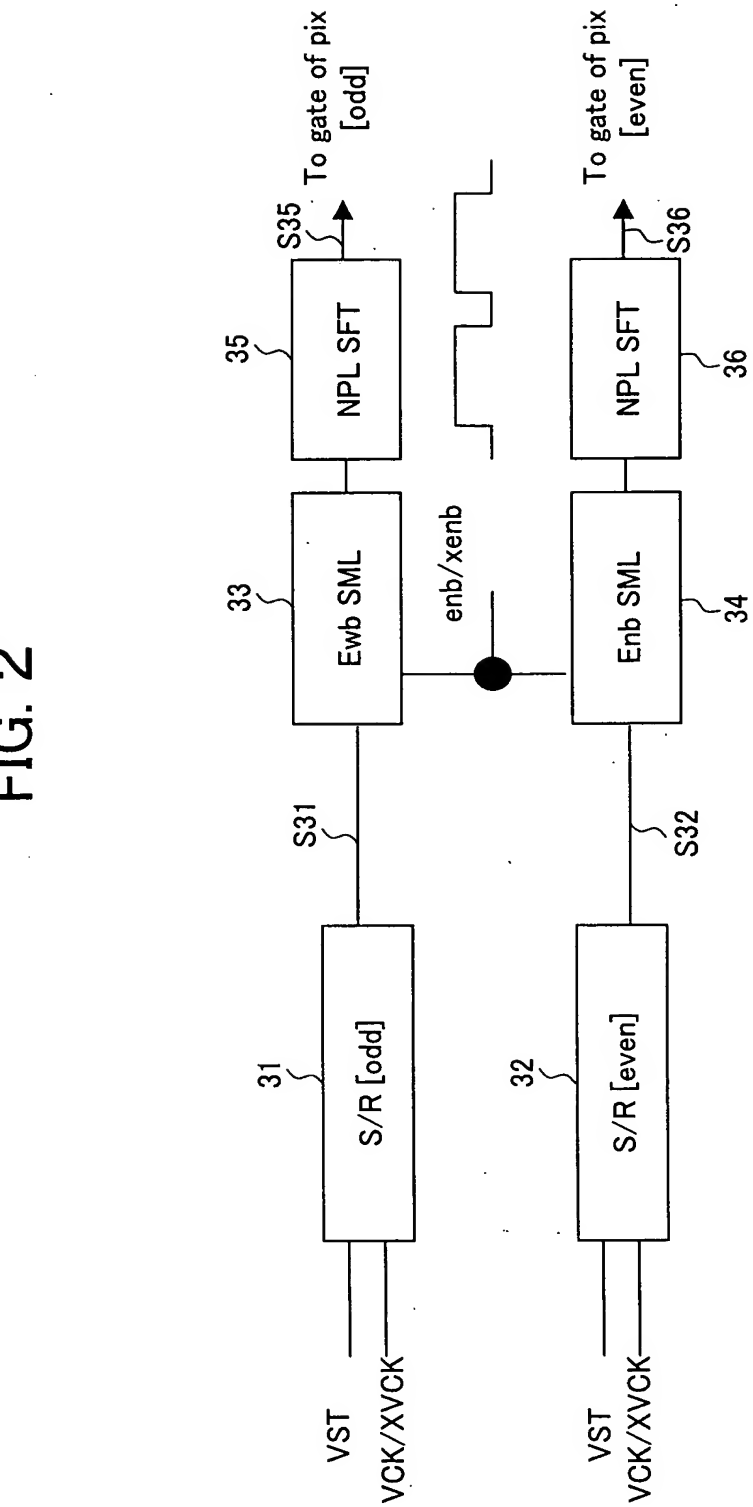


FIG. 2


VST
VCK/XVCK
S/R [odd]
31
S/R [even]
32
S31
S32
Ewb SML
33
Enb SML
34
enb/xenb
NPL SFT
35
NPL SFT
36
S35
S36
To gate of pix [odd]
To gate of pix [even]

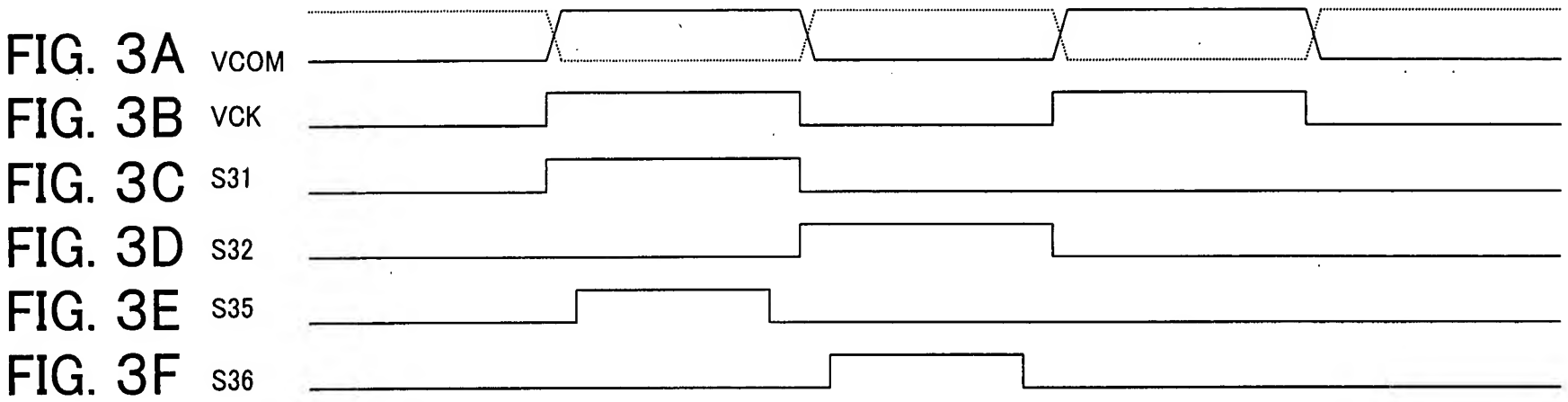


FIG. 3A VCOM
FIG. 3B VCK
FIG. 3C S31
FIG. 3D S32
FIG. 3E S35
FIG. 3F S36

FIG. 4

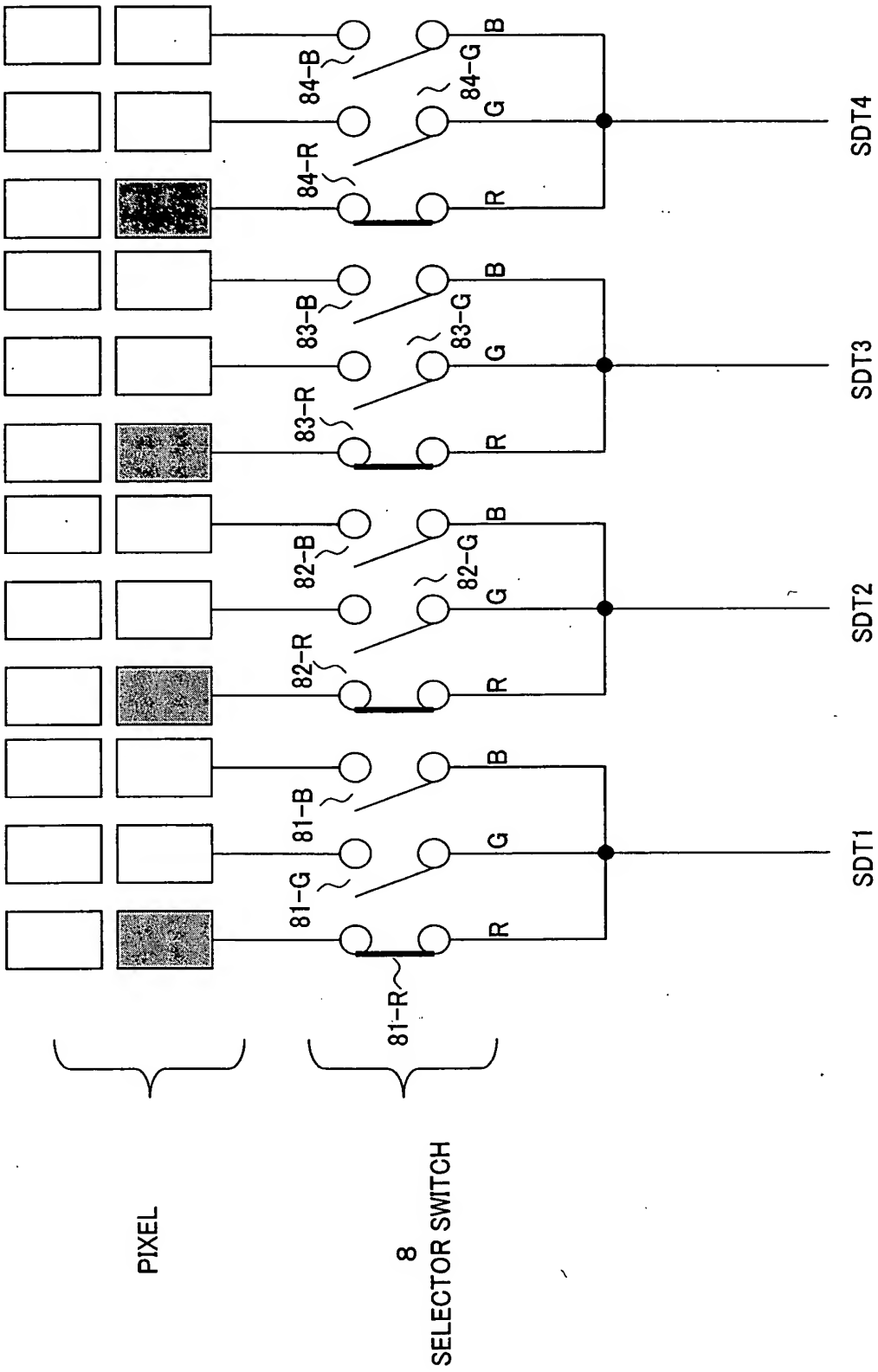

PIXEL
8
SELECTOR SWITCH
81-R
81-G
81-B
82-R
82-G
82-B
83-R
83-G
83-B
84-R
84-G
84-B
R
G
B
SDT1
SDT2
SDT3
SDT4

FIG. 5

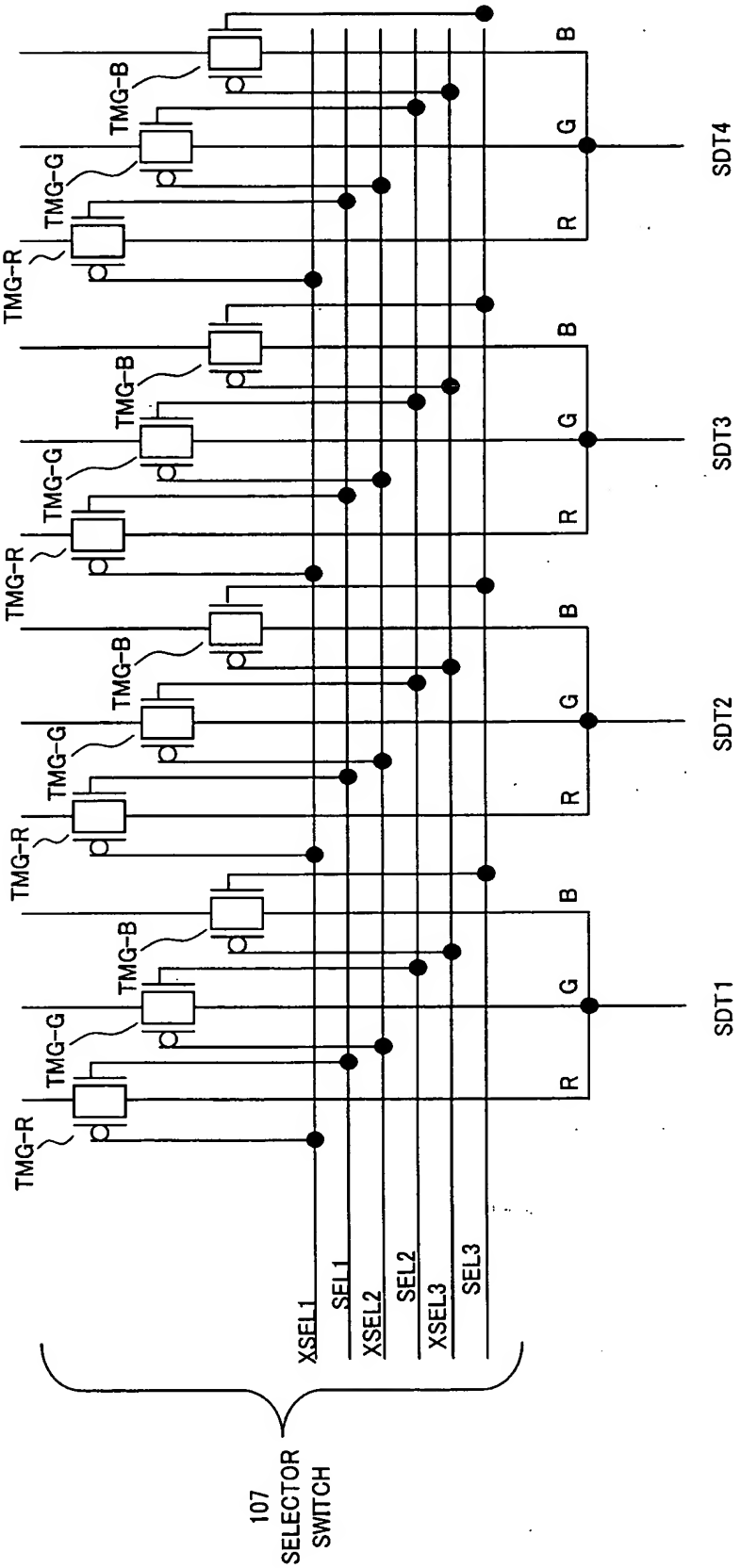

107
SELECTOR
SWITCH
XSEL1
SEL1
XSEL2
SEL2
XSEL3
SEL3
TMG-R
TMG-G
TMG-B
R
G
B
SDT1
SDT2
SDT3
SDT4

FIG. 6

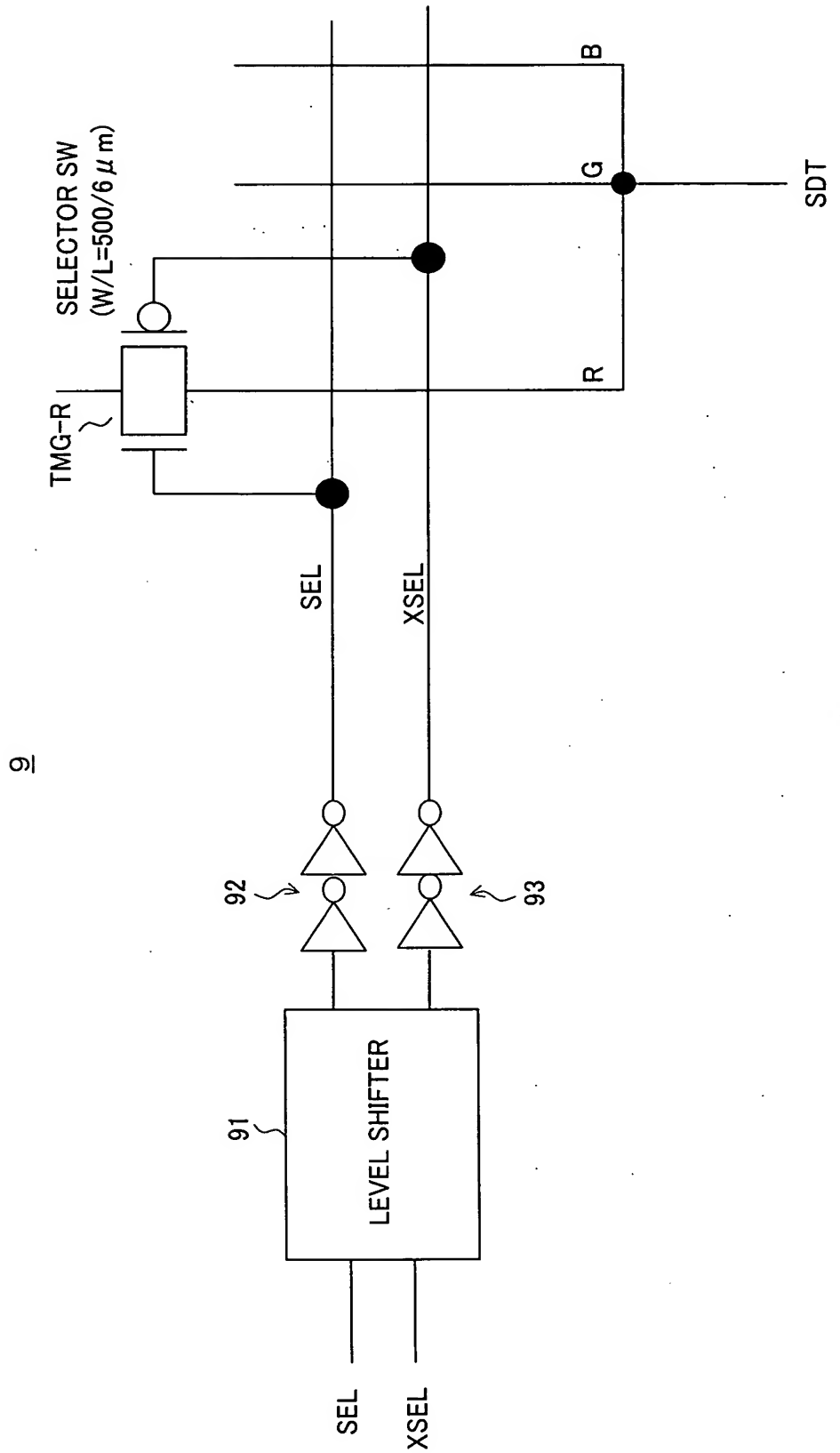

9
SELECTOR SW
(W/L=500/6 μm)
TMG-R
B
G
R
SDT
SEL
XSEL
92
93
91
LEVEL SHIFTER
SEL
XSEL

FIG. 7

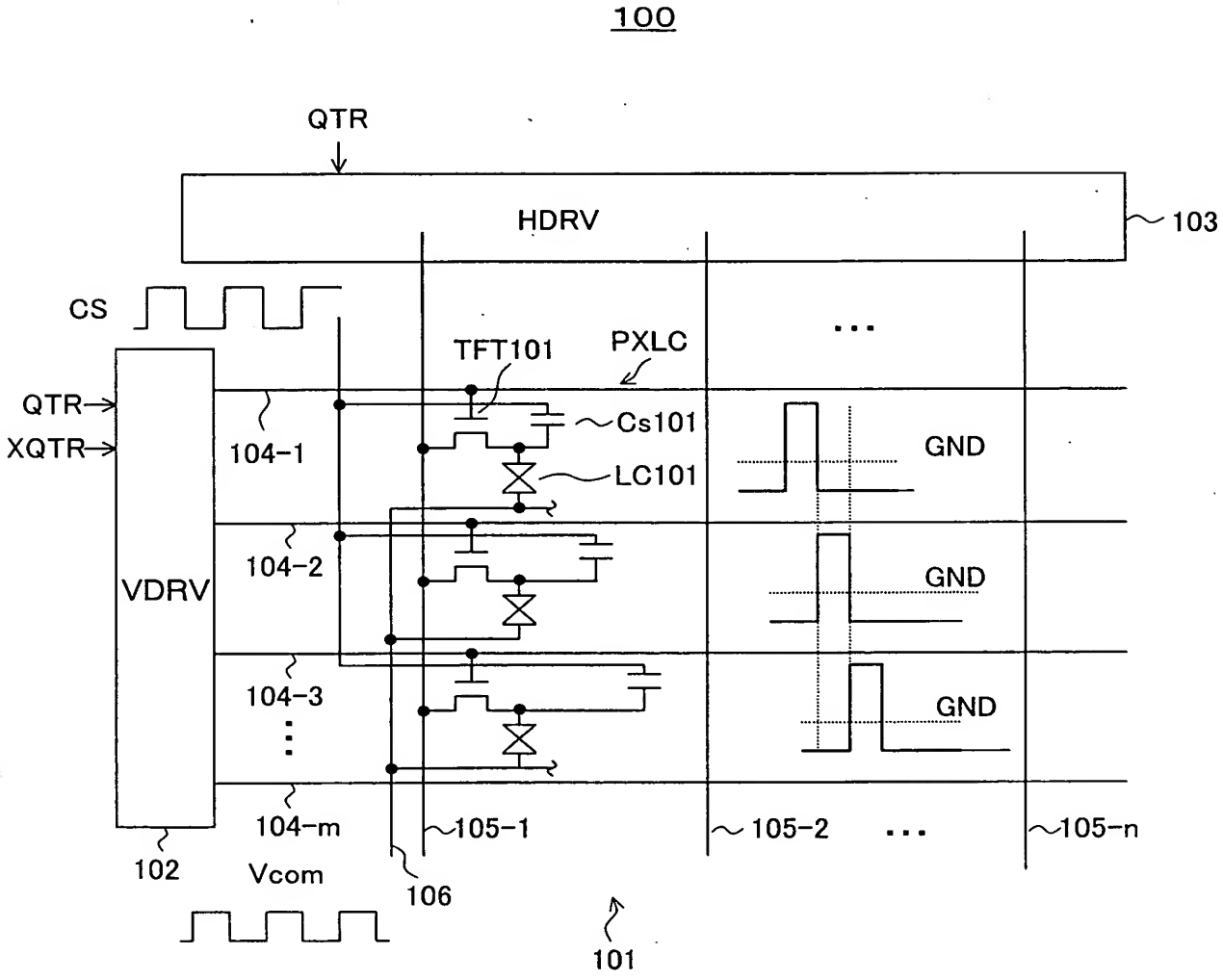

100
QTR
HDRV
103
CS
TFT101
PXLC
Cs101
LC101
GND
QTR
XQTR
VDRV
104-1
104-2
104-3
104-m
105-1
105-2
105-n
102
Vcom
106
101

FIG. 8A

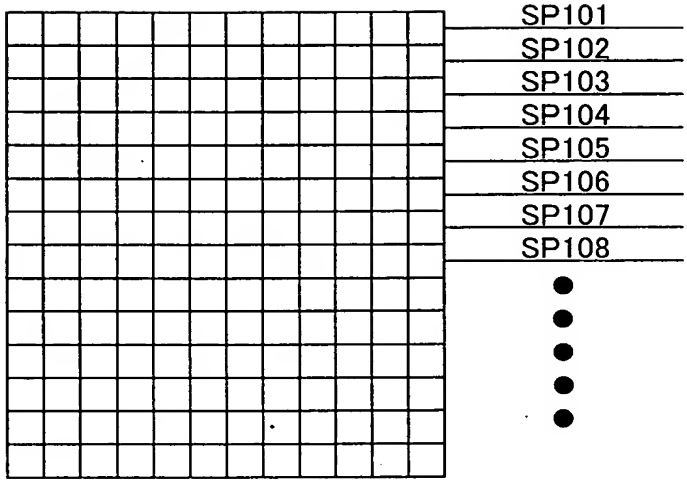


FIG. 8B

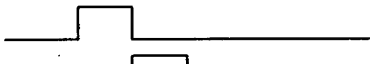


FIG. 8C

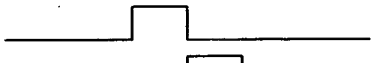


FIG. 8D

FIG. 8E

FIG. 9A

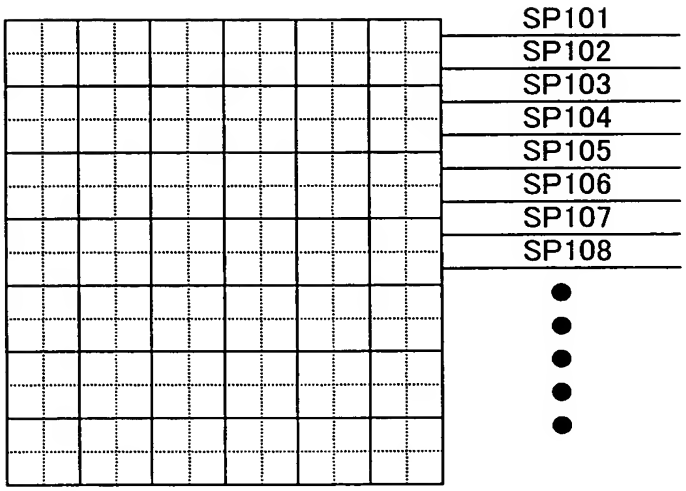


FIG. 9B SP101

FIG. 9C SP102

FIG. 9D SP103

FIG. 9E SP104

FIG. 10

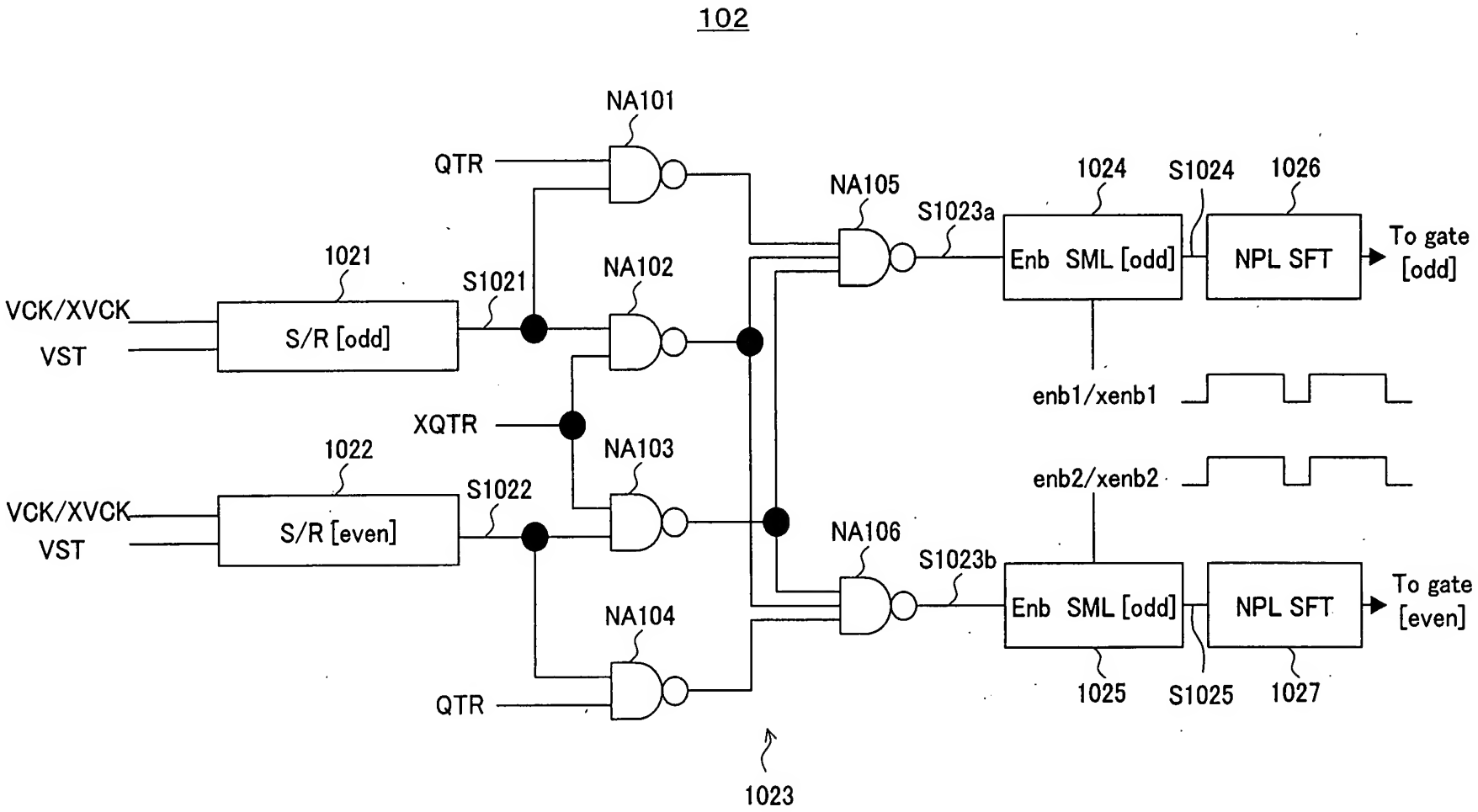

102
NA101
QTR
1021
S1021
NA102
VCK/XVCK
VST
S/R [odd]
XQTR
1022
NA103
S1022
VCK/XVCK
VST
S/R [even]
NA104
QTR
1023
NA105
S1023a
1024
S1024
1026
Enb SML [odd]
NPL SFT
To gate [odd]
enb1/xenb1
enb2/xenb2
NA106
S1023b
Enb SML [odd]
NPL SFT
To gate [even]
1025
S1025
1027

FIG. 11

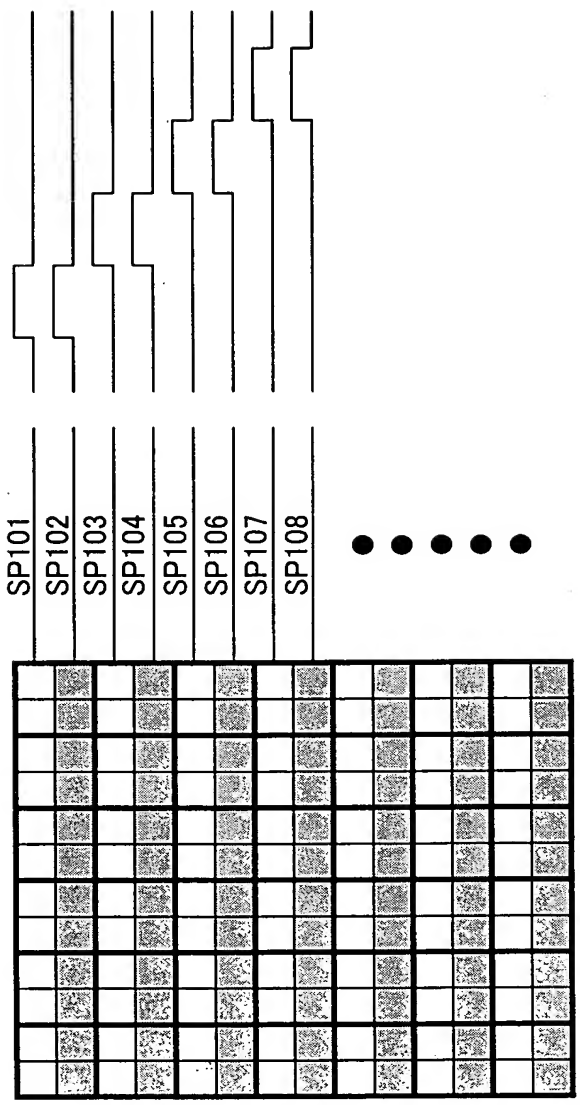


FIG. 12

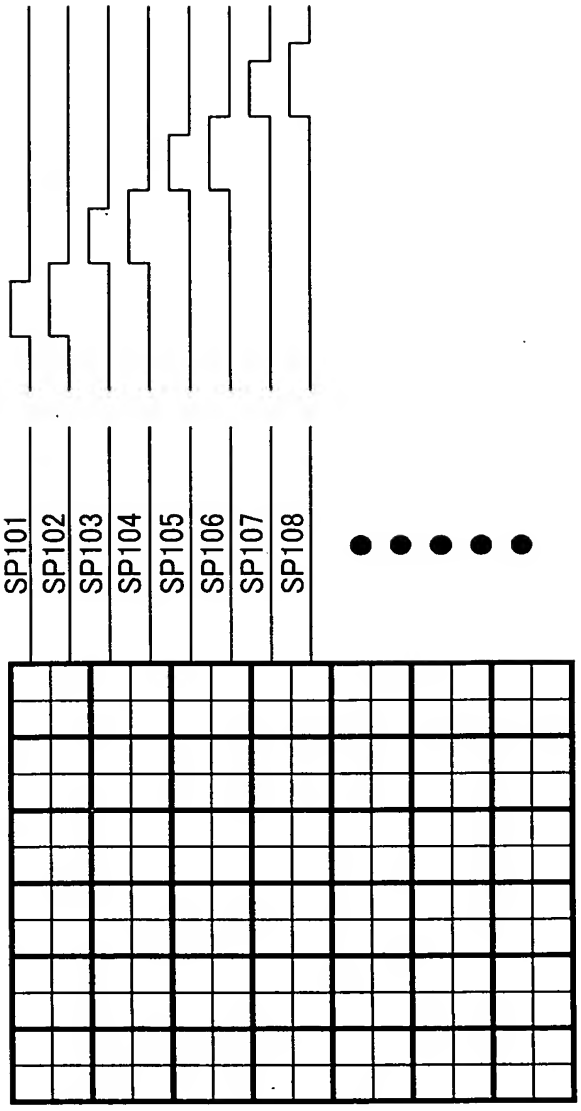


FIG. 13

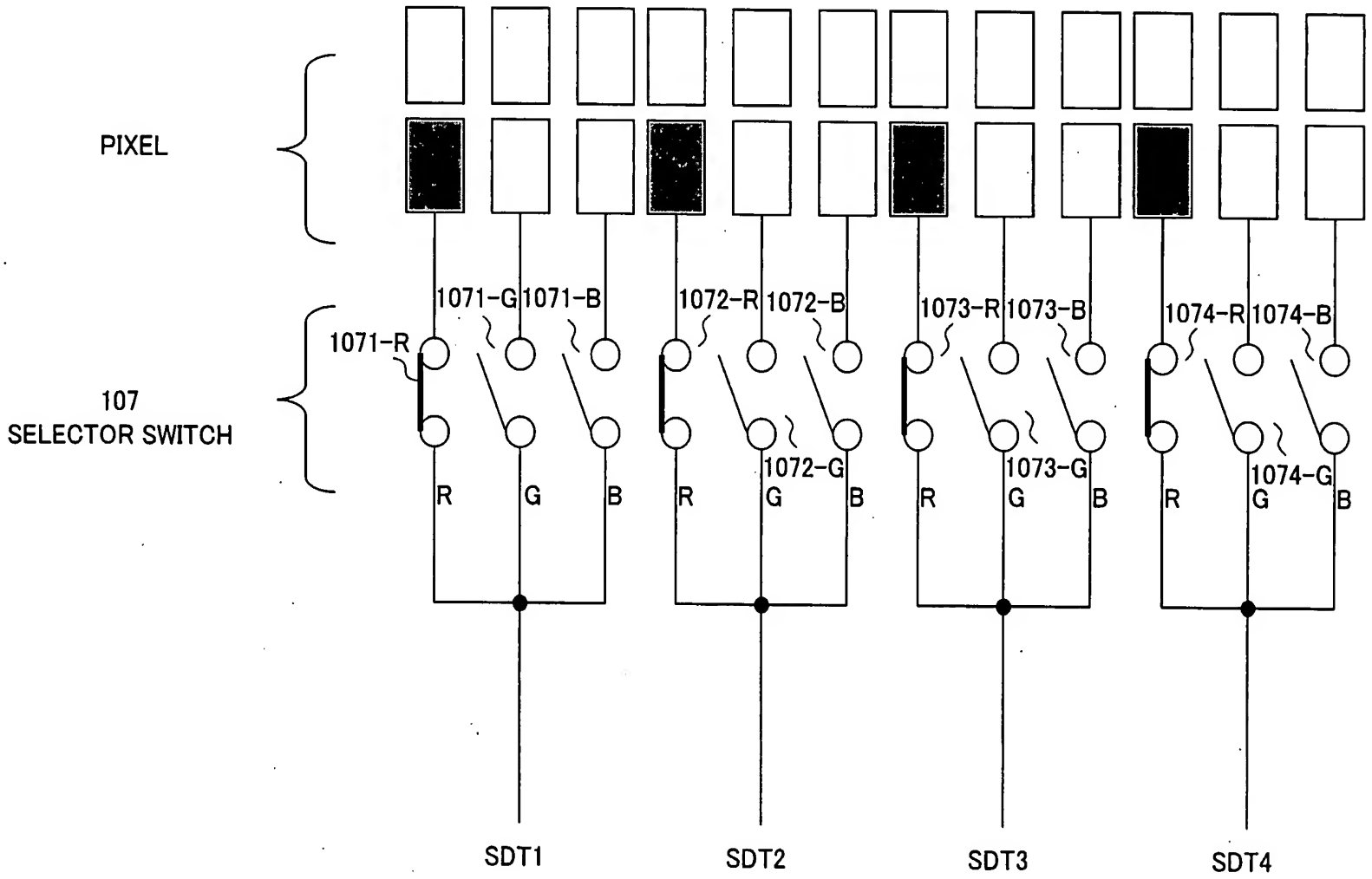

PIXEL
107
SELECTOR SWITCH
1071-R
1071-G
1071-B
1072-R
1072-B
1073-R
1073-B
1074-R
1074-B
1072-G
1073-G
1074-G
R
G
B
SDT1
SDT2
SDT3
SDT4

FIG. 14

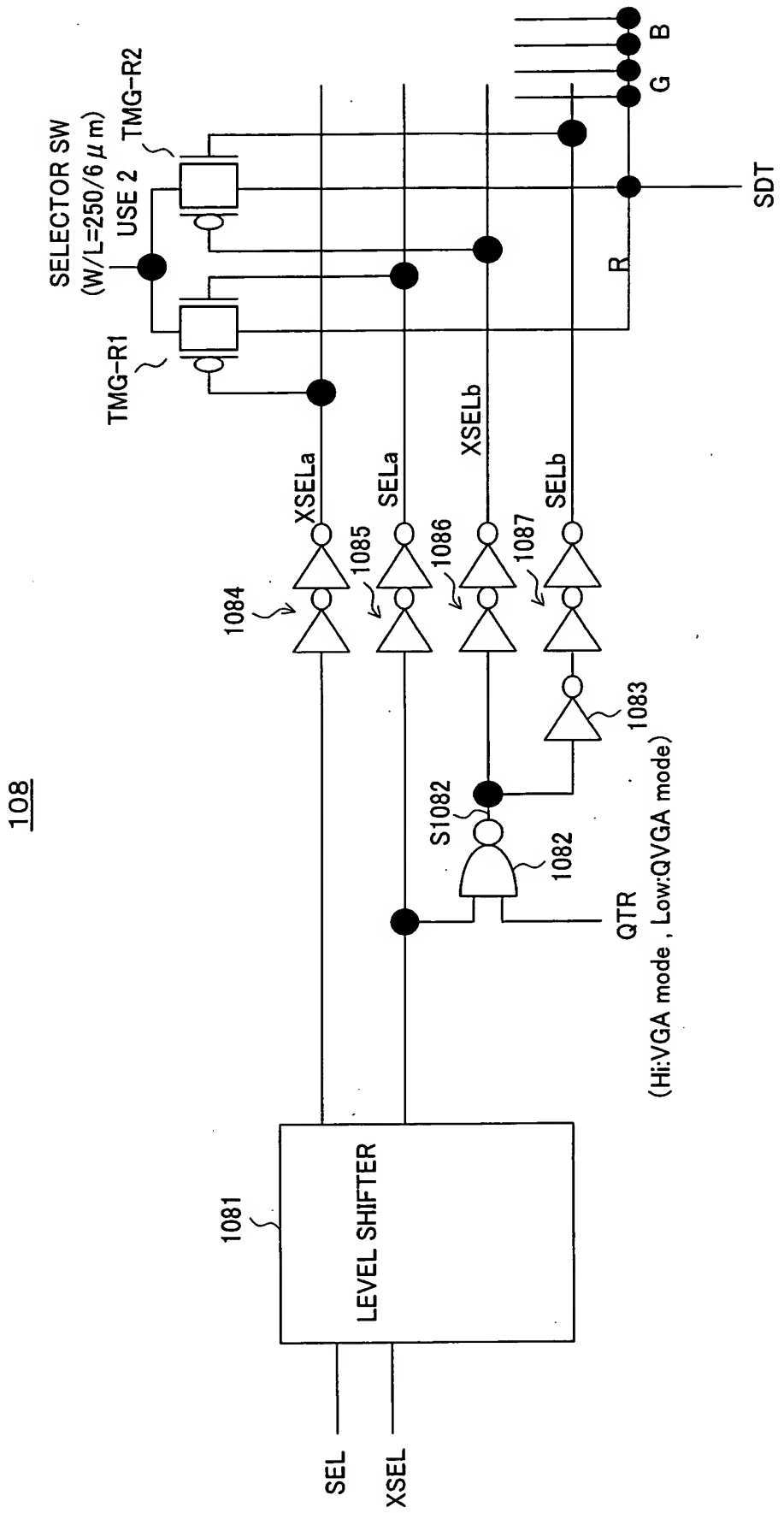
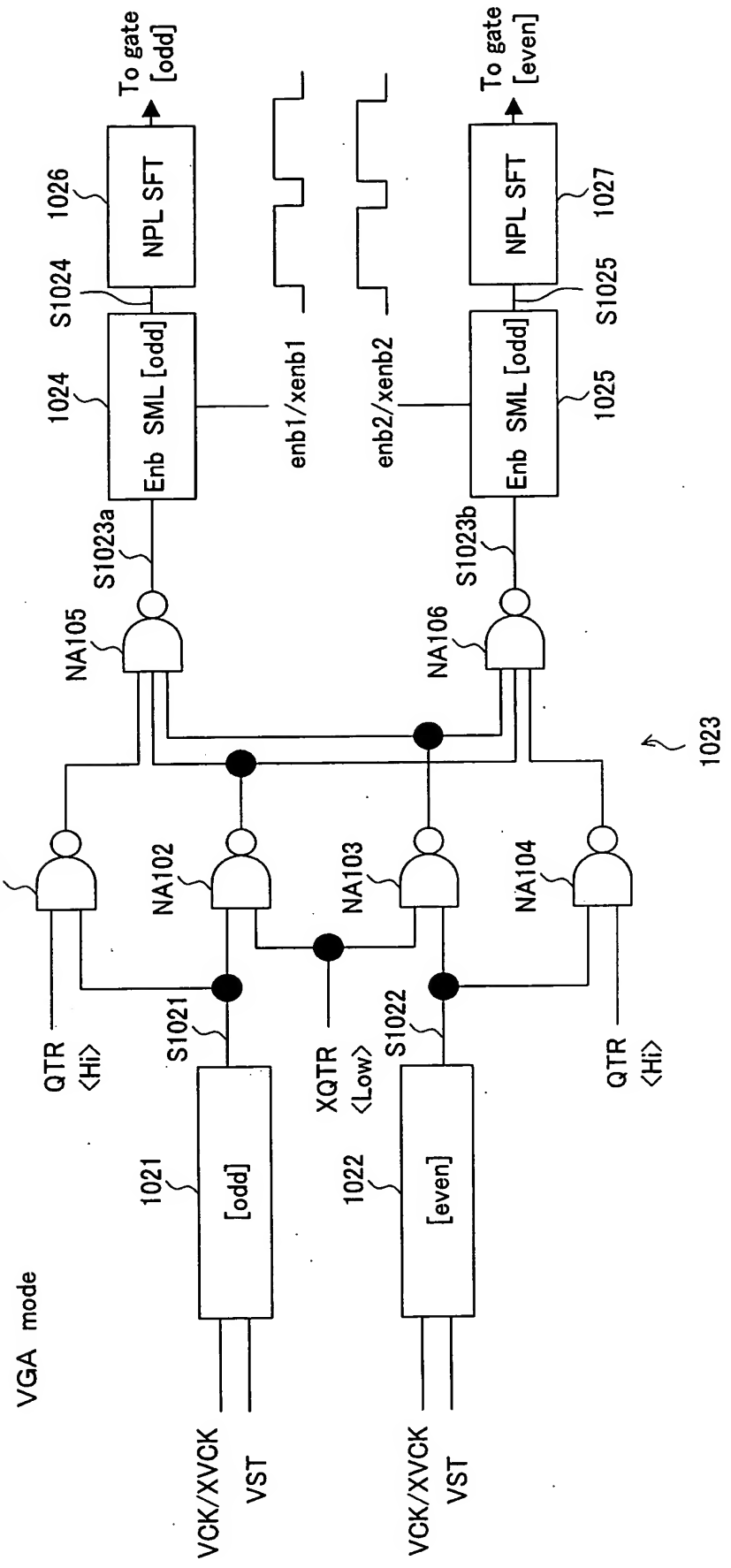

108
SEL
XSEL
1081
LEVEL SHIFTER
1082
S1082
QTR
(Hi:VGA mode , Low:QVGA mode)
1083
1084
1085
1086
1087
XSELa
SELa
XSELb
SELb
TMG-R1
SELECTOR SW
(W/L=250/6 μ m)
USE 2
TMG-R2
R
G
B
SDT

FIG. 15


VGA mode
VCK/XVCK
VST
VCK/XVCK
VST
1021
[odd]
1022
[even]
S1021
S1022
QTR
<Hi>
XQTR
<Low>
QTR
<Hi>
NA101
NA102
NA103
NA104
NA105
NA106
S1023a
S1023b
1023
1024
Enb SML [odd]
1025
Enb SML [odd]
enb1/xenb1
enb2/xenb2
S1024
S1025
1026
NPL SFT
1027
NPL SFT
To gate
[odd]
To gate
[even]

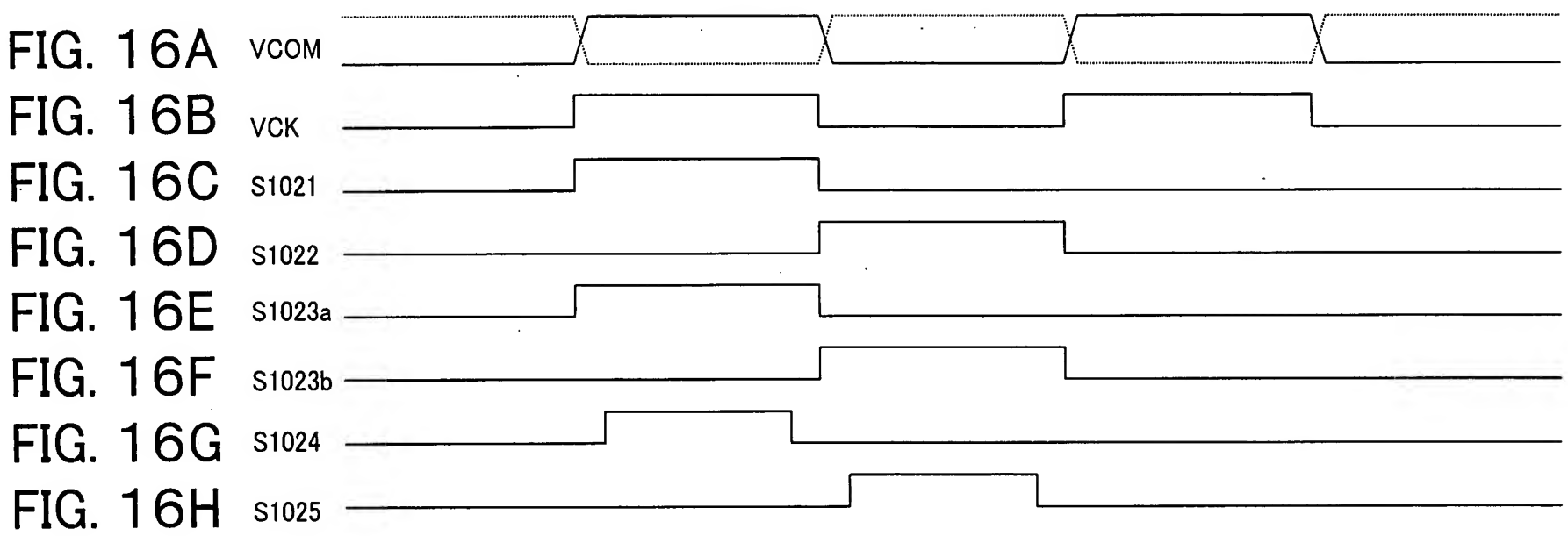
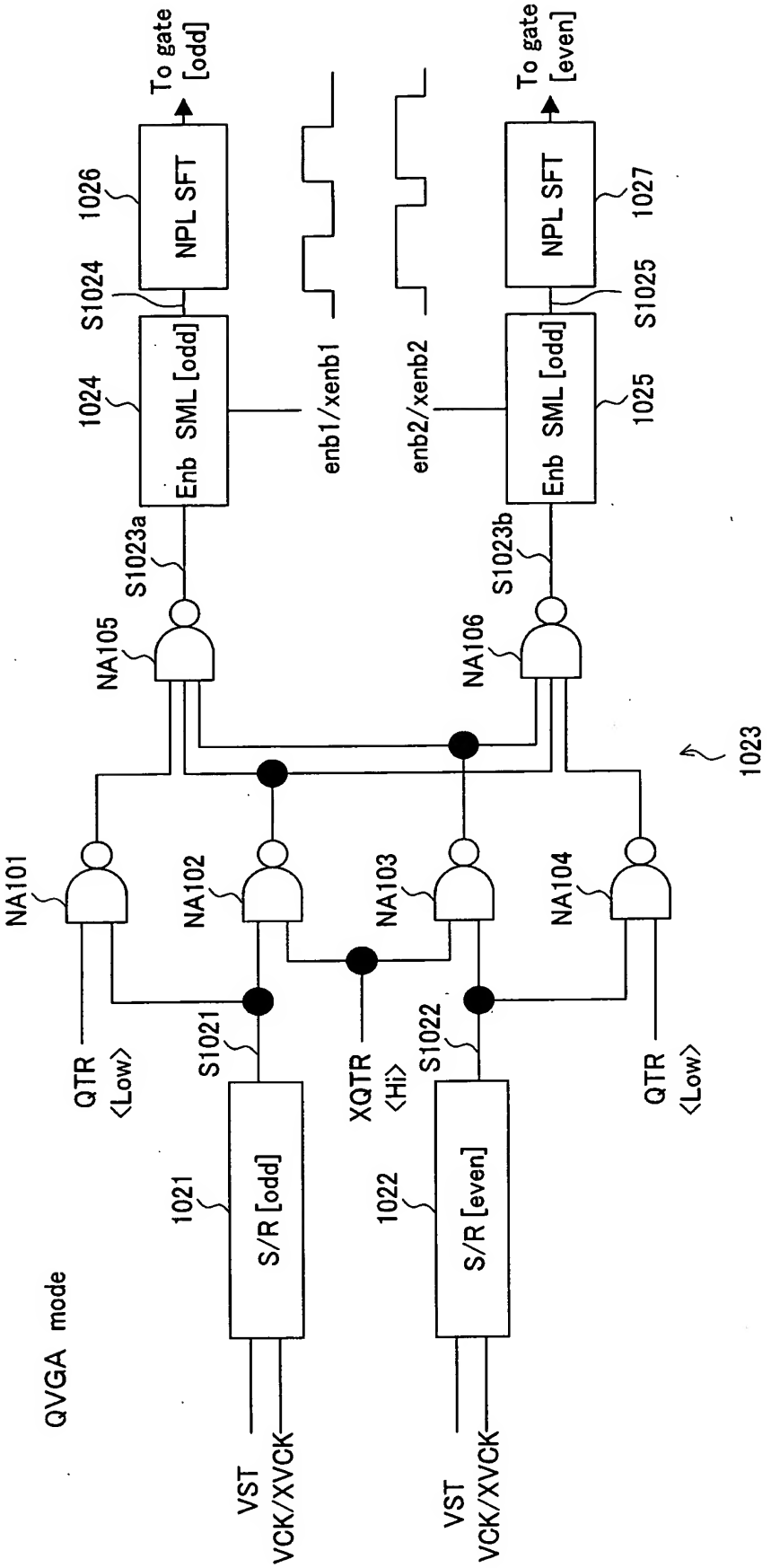


FIG. 16A
VCOM
FIG. 16B
VCK
FIG. 16C
S1021
FIG. 16D
S1022
FIG. 16E
S1023a
FIG. 16F
S1023b
FIG. 16G
S1024
FIG. 16H
S1025

FIG. 17


QVGA mode
VST
VCK/XVCK
VST
VCK/XVCK
1021
S/R [odd]
1022
S/R [even]
S1021
S1022
QTR
<Low>
XQTR
<Hi>
QTR
<Low>
NA101
NA102
NA103
NA104
NA105
NA106
S1023a
S1023b
1024
Enb SML [odd]
1025
Enb SML [odd]
S1024
S1025
1026
NPL SFT
1027
NPL SFT
To gate
[odd]
To gate
[even]
enb1/xenb1
enb2/xenb2
1023

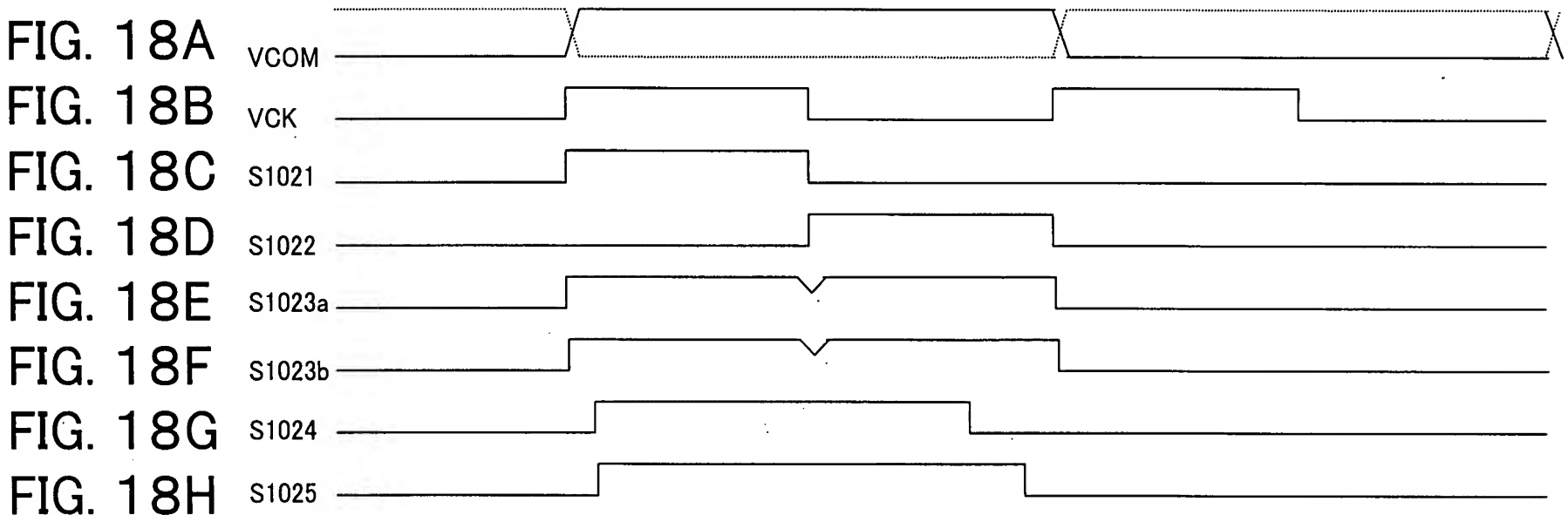


FIG. 18A
VCOM
FIG. 18B
VCK
FIG. 18C
S1021
FIG. 18D
S1022
FIG. 18E
S1023a
FIG. 18F
S1023b
FIG. 18G
S1024
FIG. 18H
S1025

FIG. 19

		VGA MODE	QVGA MODE	
			Ref CIRCUIT	LOW CONSUMPTION USE CIRCUIT
SELECTOR SW Tr SIZE	W	500 μm	500 μm	250 μm(+250 μm)
	L	6 μm	6 μm	6 μm
CONSUMED POWER		8.5mW	4.25mW	2.13mW
SIGNAL LINE WRITING τ		0.88 μsec	0.88 μsec	1.0 μsec
SELECTOR FALLING τ		0.16 μsec	0.16 μsec	0.16 μsec

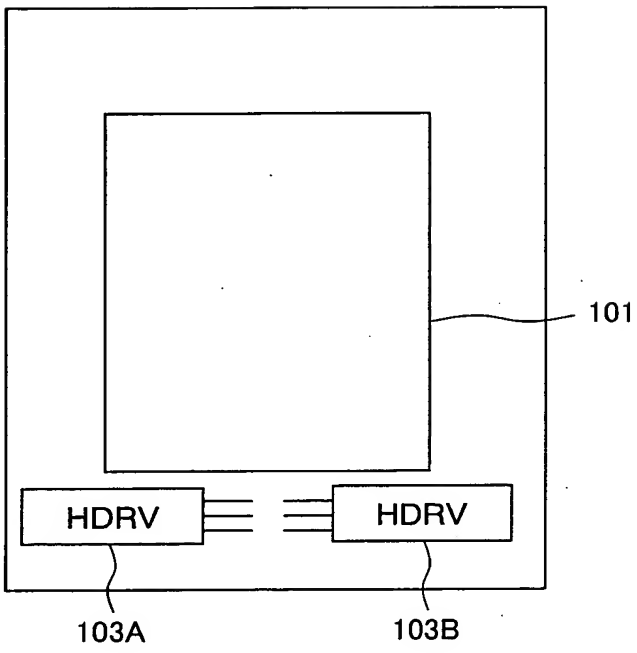



FIG. 20